For: METHOD AND COMPUTER PROGRAM PRODUCT FOR
                OFFLOADING PROCESSING TASKS FROM SOFTWARE TO
                HARDWARE

References Cited by Applicants

While the filing of Information Disclosure Statements is voluntary, the procedure is governed by the guidelines of Section 609 of the Manual of Patent Examining Procedure and 37 C.F.R. §§ 1.97 and 1.98. To be considered a proper Information Disclosure Statement, Form PTO-1449 shall be accompanied by a copy of each listed patent or publication or other item of information and a translation of the pertinent portions of foreign documents (if an existing translation is readily available to the applicant), an explanation of relevance of each reference not in the English language, and should be submitted in a timely manner as set out in MPEP Sec. 609.

Examiners will consider all citations submitted in conformance with 37 C.F.R. § 1.98 and MPEP Sec. 609 and place their initials adjacent the citations in the spaces provided on this form. Examiners will also initial citations not in conformance with the guidelines which may have been considered. A reference may be considered by the Examiner for any reason whether or not the citation is in full conformance with the guidelines. A line will be drawn through a citation if it is not in conformance with the guidelines AND has not been considered. A copy of the submitted form, as reviewed by the Examiner, will be returned to the applicant with the next communication. The original of the form will be entered into the application file.

Each citation initialed by the Examiner will be printed on the issued patent in the same manner as references cited by the Examiner on Form PTO-892.

The reference designations "A1," "A2," etc. (referring to Applicant's reference 1, Applicant's reference 2, etc.) will be used by the Examiner in the same manner as Examiner's reference designations "A," "B," "C," etc. on Office Action Form PTO-1142.

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Examiner: _____   Date Considered: 10/27/04

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Express Mail Label No. EL 656 157 120 US
Form PTO-1449
Applicant: Sanjay Anand, et al.
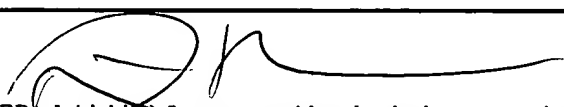Att'y Docket No.: 13768.69.1.1

Sheet 1 of 3.

Group: Unknown

For: METHOD AND COMPUTER PROGRAM PRODUCT FOR OFFLOADING PROCESSING TASKS FROM SOFTWARE TO HARDWARE

JC760 U.S. PTO
09/726082
11/29/00

INFORMATION DISCLOSURE CITATIONS MADE BY APPLICANT

U.S. Patent Documents

Examiner Initial*		Patent Number	Issue Date	Name	Class	Sub Class
⟨initials⟩	A1.	5,410,696	04/1995	Seki et al.	395	650
	A2.	5,504,903	04/1996	Chen et al.	395	700
	A3.	5,621,894	04/1997	Menezes et al.	395	200.12
	A4.	5,634,070	05/27/97	Robinson	395	800
	A5.	5,678,021	10/1997	Pawate et al.	395	431
	A6.	5,717,691	02/10/98	Dighe et al.	370	401
	A7.	5,737,520	04/1998	Gronlund et al.	395	183.15
	A8.	5,889,848	03/1999	Cookson	379	230
⟨initials⟩	A9.	5,913,028	06/1999	Wang et al.	395	200.33

Examiner: ⟨signature⟩   Date Considered: 10/27/04

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Foreign Patent Documents

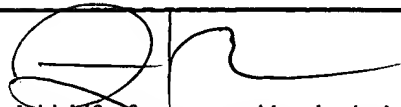| Examiner Initial*	Document Number	Publ. Date	Country or Patent Office	Class	Sub Class	Trans-lation
A10.	0778523	06/11/97	EP	---	---	Yes

Other Documents

(including author (if listed), title, relevant pages, date of publication including at least month and year).

Examiner
Initial*

A11.   Gott, Robert A., "Intelligent I/O Eases Subsystem Development," *Computer Design*, Vol. 37, No. 5, pp. 106, 108-110, May 1, 1998.

Examiner:	Date Considered: 10 27 04

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